REMARKS

Claims 1-17 are pending in the present application.

The rejection of Claim 1 under 35 U.S.C. §102(b) over Blanchard (U.S. Patent No. 2002/0125527) is respectfully traversed.

The present invention provides, *inter alia*, a semiconductor substrate comprising:

> a lightly doped substrate that contains impurities at a low concentration;
>
> a heavily doped diffusion layer which is formed over a top of the lightly doped substrate and is higher in impurity concentration than the lightly doped substrate; and
>
> an epitaxial layer which is formed over a top of the heavily doped diffusion layer and contains impurities at a lower concentration than the heavily doped diffusion layer (see Claim 1).

From the foregoing, Applicants submit that it is clear that the semiconductor substrate of the present invention is formed of three superposed layers, i.e., a lightly doped substrate, a heavily doped diffusion layer and an epitaxial layer. The heavily doped diffusion layer is formed over a top of the lightly doped substrate, and the epitaxial layer is formed over a top of the heavily doped diffusion layer. Applicants further submit that the specific relationship between these layers is neither disclosed nor suggested by Blanchard.

In the present invention, Applicants submit that the term "formed over" substantially means "entirely cover." Support for this meaning is found in the figures showing cross sectional views of the semiconductor substrates of the embodiments according to the present invention, in which a heavily doped diffusion layer entirely covers a top of the lightly doped substrate, and an epitaxial layer entirely covers a top of the heavily doped diffusion layer.

For example, in Figure 10 a heavily doped diffusion layer 9 entirely covers a top of the lightly doped substrate 5, and an epitaxial layer 10 entirely covers a top of the heavily doped diffusion layer 9. No region or part is formed in the structure of the semiconductor substrate. From this specific structure the resistivity of the epitaxial layer is uniform over the wafer.

The Examiner cites Blanchard and alleges that Figure 3 of this reference provides a semiconductor substrate "comprising:

a lightly doped substrate (25, n-type) that contains impurities at a low concentration;

a heavily doped diffusion layer (11, see paragraph# 31, figure 3) which is formed over a top of the lightly doped substrate (25) and is higher in impurity concentration than the lightly doped substrate(see paragraph# 31); and

an epitaxial layer (12) which is formed over a top of the heavily doped diffusion layer and contains impurities at a lower concentration than the heavily doped diffusion layer (see figure 3, paragraph# 31)." (see page 3 of Office Action mailed on November 15, 2005)

Contrary to Examiner's allegation, the DMOS transistor disclosed by Blanchard is structurally distinct from the semiconductor substrate of the present invention. Specifically, the heavily doped diffusion layer 11 appearing in Figure 3 of Blanchard is a *buried* region, and formed on a *portion* of the substrate 25. In other words, the heavily doped diffusion layer 11 disclosed by Blanchard is not formed over the substrate 25. Therefore, it is clear that the heavily doped diffusion layer 11 disclosed by Blanchard does not correspond to the heavily doped diffusion layer recited in claim 1 of the present application which is formed over a top of the lightly doped substrate and is higher in impurity concentration than the lightly doped substrate.

Further, it should be noted that Blanchard discloses a semiconductor device formed in a semiconductor substrate, not a semiconductor substrate *per se*. In the device shown in

Figure 3 of Blanchard, the semiconductor substrate is basically formed of *two* superposed layers: a p-type substrate 25 and a semiconductor layer, unnumbered, formed over the p-type substrate. Therefore, Blanchard does not disclose a semiconductor substrate formed of *three* superposed layers as recited in claim 1 of the present application.

The Examiner is reminded that in order for a reference to anticipate an invention, the reference "must teach every element of the claim" (MPEP §2131). As such, Applicants submit that Blanchard fails to anticipate the claimed invention.

In view of the foregoing, Applicants request withdrawal of this ground of rejection.

The rejection of Claims 10, 11, and 13 under 35 U.S.C. §102(b) over Admic Jr. (U.S. Patent No. 6,124,179) is respectfully traversed.

The present invention provides, *inter alia*, a semiconductor substrate comprising:

a heavily doped diffusion layer which is formed over a top of a lightly doped substrate and is higher in impurity concentration than the lightly doped substrate, the lightly doped substrate being removed at a final stage of a process; and

an epitaxial layer which is formed over a top of the heavily doped diffusion layer and contains impurities at a lower concentration than the heavily doped diffusion layer, wherein an impurity diffusion layer for forming a semiconductor device is formed in the epitaxial layer (see Claim 10).

Applicants submit that Admic Jr. does not disclose a semiconductor substrate formed of three superposed layers for the same reasons that Blanchard is deficient. The Examiner attempts to disregard the clear difference noting that the presence and subsequent removal of the lightly doped substrate at the final stage of processing is not relevant to the final product.

Applicants wish to draw the Examiner's attention to *In re Thorpe*, 227 USPQ 964 (Fed. Cir. 1985), which provides: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claims is unpatentable even though the prior product was made by a different process."

There are two important aspects to the foregoing. *First*, the products must be identical or an obvious variant thereof. *Second*, patentability of a product may not depend on its method of production, but the method of production cannot be disregarded if that method provides a distinct structure or product. Indeed, the Board and the Courts have said as much in two decisions that are set forth in MPEP §2113, which states in relevant part:

> "The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where... the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g. *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979)... The Board stated that the dispositive issue is whether the claimed factor exhibits any unexpected properties compared with the factor disclosed by the prior art." (citing *Ex parte Gray*, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989)

Applicants submit that the foregoing is particularly relevant to the present application. The methods disclosed by the cited art of record fail to recite the presence and subsequent removal of the lightly doped substrate at the final stage of processing. This deficiency is significant in that the structure of the semiconductor substrate requires that each layer be completely superposed on the layer below it. Since the impurity concentration of the lightly doped substrate 100 can be set so low that such outward diffusion of impurities contained in the substrate as affects the resistivity of the epitaxial layer 3 will not occur. For this reason, the substrate can be fabricated at a low cost in comparison with conventional heavily doped

substrates (see page 15, line 24 to page 16, line 3). Moreover, since the heavily doped diffusion layer 2 is formed by means of diffusion techniques, a uniform resistivity distribution can be obtained in a lot without being affected by segregation occurred at the crystal growth time in the formation of conventional heavily doped substrates (see page 16, lines 6-12).

Based on the foregoing, it is clear that the present method imparts a structure advantage (i.e., uniform resistivity distribution) as compared to methods conventionally employed (e.g., Adamic Jr.).

In view of the foregoing, Applicants request withdrawal of this ground of rejection.

The rejection of Claims 2-5 and 12 under 35 U.S.C. 103(a) over Blanchard (U.S. Patent No. 2002/0125527) or Admic Jr. (U.S. Patent No. 6,124,179) in view of the applicants alleged admission of the Prior Art on pages 1-4 of the present specification is respectfully traversed.

Blanchard and Admic Jr. are discussed above and each fails to disclose or suggest a semiconductor substrate meeting the limitations of independent Claims 1 and 10. The alleged admission of the Prior Art on pages 1-4 of the present specification is cited as showing that lightly doped substrates contains phosphorus or boron and that the resistance of the epitaxial layer is 10 Ωcm or less. However, this citation fails to compensate for the aforementioned deficiencies in the disclosures of Blanchard and Admic Jr. Therefore, Applicants submit that the combined disclosures of Blanchard or Admic Jr. with the alleged admission of the Prior Art on pages 1-4 of the present specification fails to render the present invention obvious.

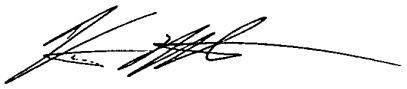
According, withdrawal of this ground of rejection is requested.

Applicants submit that the present application is now in condition for allowance.

Early notice to this effect is earnestly solicited.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.
Norman F. Oblon



Vincent K. Shier, Ph.D.
Registration No. 50,552

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413-2220
(OSMMN 08/03)